said at least one second trench includes a trench formed in said predetermined direction,

said first semiconductor region includes a first section formed in a vicinity of said at least one first trench and a second section extended from said first section in such a direction as to go away from said at least one first trench, and

said first main electrode is directly formed on said second section to carry out an electrical connection to said first semiconductor region.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-13 and 21-32 are pending in the present application. Claims 1 and 3 have been amended by the present amendment.

In the outstanding Office Action, the Information Disclosure Statement (IDS) filed on December 27, 2002, was objected to because the references are not identified by the inventor and a PTO-1449 or PTO/SB/08A form is missing; Claims 3-5 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite; Claims 1-11 and 21-32 were rejected under 35 U.S.C. § 103(a) as obvious over Takahashi (U.S. Patent No. 5,960,264, herein "Takahashi '264") in view of Osawa (U.S. Patent No. 6,501,129 B2); Claim 12 was rejected under 35 U.S.C. § 103(a) as obvious over Takahashi '264 in view of Osawa and Uenishi et al (U.S. Patent No. 5,894,149, herein "Uenishi"); and Claim 13 was rejected under 35 U.S.C. § 103(a) as obvious over Takahashi '264 in view of Osawa and Takahashi (U.S. Patent No. 6,001,678, herein "Takahashi '678").

Since the present amendment places the claims in better form for consideration on appeal by amending Claims 1 and 3 to more clearly recite novel features of the present

invention, entry of this amendment under 37 C.F.R. § 1.116 is believed to be in order and it is therefore respectfully requested.

Regarding the objection to the IDS filed on December 27, 2002, Applicant addresses the two reasons for objection separately.

First, the outstanding Office Action objects to the filed IDS because the references listed on the IDS are not identified by their inventor. Applicant respectfully submits that each of the references listed on the IDS is identified by a serial number and a filing date. It is respectfully submitted that this information alone allows a unique identification of each U.S. patent application even if the name of the inventor has been omitted. In addition, the transmission form accompanying the filed IDS specifically states "[a]ttached is a list of applicant's pending application(s)." In view of this statement and the fact that there is only one Applicant in this application, it is respectfully submitted that the inventor is clearly identified. In addition, Applicant notes that under 37 CFR 1.41(b) the term "applicant" "refers to the inventor or joint inventors who are applying for a patent." Therefore, the references listed on the filed IDS are clearly identified by the inventor of this application.

Second, the outstanding Office Action also objects to the IDS filed on December 27, 2002, because "there is no PTO-1449 or PTO/SB/08A or its equivalent."[2]

Applicant respectfully submits that MPEP § 609 only encourages the applicant using the PTO-1449 or PTO/SB/08A forms.[3] Moreover, MPEP at § 609 ¶ III C(2) states "[i]f the citations are submitted on a list other than on a form PTO-1449 or PTO/SB/08A and 08B, the examiner may write 'All considered' and his or her initials to indicate that all citations have been considered." Therefore, it is respectfully submitted the list of references filed comply

[2] Outstanding Office Action, page 2, line 11.
[3] See MPEP § 609 ¶ III, A(1), last five lines, stating "[u]se of either form PTO-1449, Information Disclosure Citation, or PTO/SB/08A and 08B, Information Disclosure Statement, to list the documents is encouraged."

with the patent rules. Accordingly, it is respectfully requested the IDS filed on December 27, 2002, be considered and this objection be withdrawn.

In response to the rejection of Claims 3-5 under 35 U.S.C. § 112, second paragraph, Claim 3 has been amended to clarify features recited therein, as shown in the marked-up copy. Further, Applicant respectfully submits that considering Claims 3-5 as a whole "in light of the specification"[4] and as shown in a non-limiting example in Figure 3, a predetermined direction of a trench 7 is shown as a horizontal direction, and therefore the predetermined direction is not indefinite. Thus, it is respectfully submitted that Claims 3-5 comply with the requirements of 35 U.S.C. § 112, second paragraph. Accordingly, it is respectfully requested that this rejection be withdrawn.

Turning now to the rejection on the merits of the pending claims, independent Claim 1 has been amended to more clearly recite that a bottom part of an external wall of at least one second trench is in direct contact with a region of a second conductivity type. Amended Claim 1 finds support in Figures 1, 2, 4, 5, 7, 8, 10, 11, 18, 19 and 20 and in the specification at least at page 21, lines 1-6. It is believed no new matter has been added.

More specifically, amended Claim 1 is directed to a semiconductor device having a first semiconductor layer of a first conductivity type, a second semiconductor layer of a second conductivity type, a third semiconductor layer of the second conductivity type, and a fourth semiconductor layer of the first conductivity type. These layers are formed in this order one over the other. Further, the semiconductor device has at least one first trench and at least one second trench arranged to penetrate through at least the fourth semiconductor layer from a surface of the fourth semiconductor layer. In addition, a first material serving as a control electrode is buried in the at least one trench, a second material not being a control

[4] Id., § 2173.05(b).

electrode is formed in the at least one second trench, and a bottom part of an external wall of the at least one second trench is in direct contact with a region of the second conductivity type.

In a non-limiting example, Figure 1 shows the first semiconductor layer 1, the second semiconductor layer 3, the third semiconductor layer 4, and the fourth semiconductor layer 5. The at least one first trench 7 and the at least one second trench 11 penetrate through at least the fourth semiconductor layer 5 from a surface of the fourth semiconductor layer 5 and a bottom part of an external wall of the at least one second trench 11 is in direct contact with a region 3 of the second conductivity type.

Providing the semiconductor device of the pending claims with a first material in at least one first trench, a second material that is not a control electrode in at least one second trench, and a bottom part of an external wall of the at least one second trench in direct contact with a region of a second conductivity type advantageously decreases an ON-state voltage, maintains a breakdown voltage, and reduces a gate capacity of the semiconductor device.[5]

Turning to the applied art, Takahashi '264 shows in Figure 3 an insulated gate semiconductor device having a control electrode 49 in each trench. Therefore, Takahashi '264 does not teach or suggest a second material being formed in at least one second trench such that the second material is not a control electrode.

Further, the outstanding Office Action recognizes at page 4, lines 18-20, that Takahashi '264 "fails to disclose ... a second material formed in said at least one second trench, the second material not being a control electrode."

Osawa is asserted in the outstanding Office Action for teaching a second material formed in at least one second trench and not being a control electrode.[6] Osawa shows in

[5] Specification, page 23, lines 4-21.
[6] Outstanding Office Action, page 4, lines 21-26.

Figure 5 a first material 38 and a second material 30 buried in first and second trenches, respectively, but Osawa is silent whether the second material 30 is not a control electrode. The outstanding Office Action refers to MOSFET Figure 1 of Osawa, but the following discussion refers to the IGBT shown in Figure 5 of Osawa.

Osawa shows in Figure 5 that a whole bottom part of an external wall of the second trench 30 is in direct contact with a P-type region 39, and this structure is imbedded in an N-type drain layer 36. By forming the P-type region 39 on the bottom part of the external wall of the second trench 30 and both the P-type region 39 and the second trench 30 imbedded in the N-type drain layer 36, the device of Osawa has the disadvantage of increasing an ON-state voltage compared to a similar device in which the P-type region 39 is not present.

More specifically, in an ON-state of the claimed device, when a voltage is applied to a control gate and a current flows, a hole is injected from a back face of a P-type substrate 1 and a carrier density of an N-type layer 3 is increased, such that the ON-state voltage is decreased. However, in the device shown in Figure 5 of Osawa, because the P-type region 39 surrounds the bottom part of the external wall of the second trench 30 and because the P-type region 39 is deeper than the second trench 30, a hole injected from a P-type substrate 311 is attracted to a P-type layer 35 having a higher potential. As a consequence, the hole escapes to the source electrode 31 through the P-type region. Accordingly, the device of Osawa does not decrease the ON-state voltage.

Further, the device shown in Figure 5 of Osawa is designed to achieve an extended depletion layer. For this scope, the P-type region 39 needs to be connected to the P-type base layer 35, which further supports the above argument.

In addition, Osawa states at column 6, lines 40-51, that the P-type impurity diffusion layer 9 shown in Figure 1 is formed "on the side wall and the bottom of that portion of the contact trench [10]" and this specific arrangement of the P-type layer 9 and the second trench

10 "causes the depletion layer [13] to grow in a direction perpendicular to the gate trench during application of the reverse bias."[7] Therefore, it is critical in Osawa to have the second trench 30 working in tandem with the P-type region 39, and this synergy requires the P-type region 39 to directly contact the bottom part of the external wall of the second trench 30.

Thus, even if Takahashi '264 is considered in the outstanding Office Action as showing first and second trenches, it is respectfully submitted that one of ordinary skill in the art, absent hindsight, would not select only the second material of Osawa to fill the second trench in Takahashi '264 because none of the trenchs in Takahashi '264 is surrounded by a P-type region, as required by Osawa.

In addition, the reason for combining the applied references set forth in the outstanding Office Action, i.e., to improve a breakdown voltage, is greatly outweighed by a reason not to combine the applied references because of the degrading in the ON-state voltage produced by the second material of Osawa. Thus, it is respectfully submitted that one of ordinary skill in the art would not combine the applied references to improve a breakdown voltage to the expense of degrading the ON-state voltage.

Accordingly, it is respectfully submitted that amended Claim 1 and each of the claims depending therefrom patentably distinguish over Takahashi '264 in view of Osawa.

Regarding the rejection of Claim 12 under 35 U.S.C. § 103(a) as obvious over Takahashi '264 in view of Osawa and Uenishi, that rejection is respectfully traversed.

Uenishi is asserted in the outstanding Office Action at page 8, lines 17-21, for teaching an electrode formed on a conductive region 18 as shown in Figure 42. However, Uenishi does not overcome the deficiencies discussed above in Takahashi '264 and Osawa.

[7] Osawa, column 7, lines 2-9.

Accordingly, it is respectfully submitted that Claim 12 depending indirectly on independent Claim 1, which is believed to be allowable, patentably distinguishes over the applied art.

Regarding the rejection of Claim 13 under 35 U.S.C. § 103(a) as obvious over Takahashi '264 in view of Osawa and Takahashi '678, that rejection is respectfully traversed.

Takahashi '678 is asserted in the outstanding Office Action at page 9, lines 11-15, for teaching a sixth layer 61 of a second conductivity type as shown in Figure 12. However, Takahashi '678 does not overcome the deficiencies discussed above in Takahashi '264 and Osawa. Accordingly, it is respectfully submitted that Claim 13 depending indirectly on independent Claim 1, which is believed to be allowable, patentably distinguishes over the applied art.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Registration No. 25,599
Eckhard H. Kuesters
Registration No. 28,870
Attorneys of Record

22850

Tel.: (703) 413-3000
Fax: (703) 413-2220
GJM/EHK/RFF/cja
I:\atty\Rff\21s\215551\215551US-am5.doc

Marked-Up Copy
Serial No: 09/986,277
Amendment Filed on: June 6, 2003

IN THE CLAIMS

Please amend Claims 1 and 3 as follows:

--1. (Twice Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

a second semiconductor layer of a second conductivity type formed on the first major surface of said first semiconductor layer;

a third semiconductor layer of the second conductivity type formed on said second semiconductor layer;

a fourth semiconductor layer of the first conductivity type formed on said third semiconductor layer;

at least one first trench and at least one second trench arranged to penetrate through at least said fourth semiconductor layer from a surface of said fourth semiconductor layer such that a bottom part of an external wall of said at least one second trench is in direct contact with a region of the second conductivity type;

a first semiconductor region of the second conductivity type selectively formed in said surface of said fourth semiconductor layer vicinal to said at least one first trench;

a first insulating film formed on an internal wall of said at least one first trench;

a first material serving as a control electrode buried in said at least one first trench and formed on said first insulating film;

a second material formed in said at least one second trench, the second material not being a control electrode;

a first main electrode electrically connected to said second material formed in said at least one second trench and to at least a part of said first semiconductor region and formed over a surface of said fourth semiconductor layer; and

a second main electrode formed on the second major surface of said first semiconductor layer.

3. (Twice Amended) The semiconductor device according to claim 1, wherein

said at least one first trench includes a trench formed in a predetermined direction along [said first major] a surface of said [first] fourth semiconductor layer,

said at least one second trench includes a trench formed in said predetermined direction,

said first semiconductor region includes a first section formed in a vicinity of said at least one first trench and a second section extended from said first section in such a direction as to go away from said at least one first trench, and

said first main electrode is directly formed on said second section to carry out an electrical connection to said first semiconductor region.--